We Claim:

1. An MRAM configuration, comprising:

word lines;

bit lines running at a distance from said word lines;

first select lines;

second select lines; and

a multiplicity of memory cells disposed in a memory matrix form, said memory cells containing MTJ layer sequences and selection transistors having gates and drain-source paths, said MTJ layer sequences in each case disposed between said word lines and said bit lines, said selection transistors connected to said select lines at said gates for reading from said memory cells, said MTJ layer sequences connected to said second select lines, in a respective one of said memory cells a respective MTJ layer sequence and a respective drain-source path of a respective one of said selection transistors in each case lie parallel to one another, so that said second select lines being formed by said drain-source paths of said selection transistors lying in series with one another.

2. The MRAM configuration according to claim 1, further comprising selection transistors, and each of said second select lines of a chain of said memory cells in said memory matrix lies in series with a separate one of said selection transistors.

3. The MRAM configuration according to claim 1, wherein said gates of said selection transistors are connected to said first select lines.

4. The MRAM configuration according to claim 1, wherein said memory cells have a minimum dimension being 4 F^2 where F denotes a minimum feature size of a technology used.

5. The MRAM configuration according to claim 1, wherein said first select lines are routed above said gates of said selection transistors.

6. The MRAM configuration according to claim 4, wherein said first select lines and said bit lines run parallel to one another.